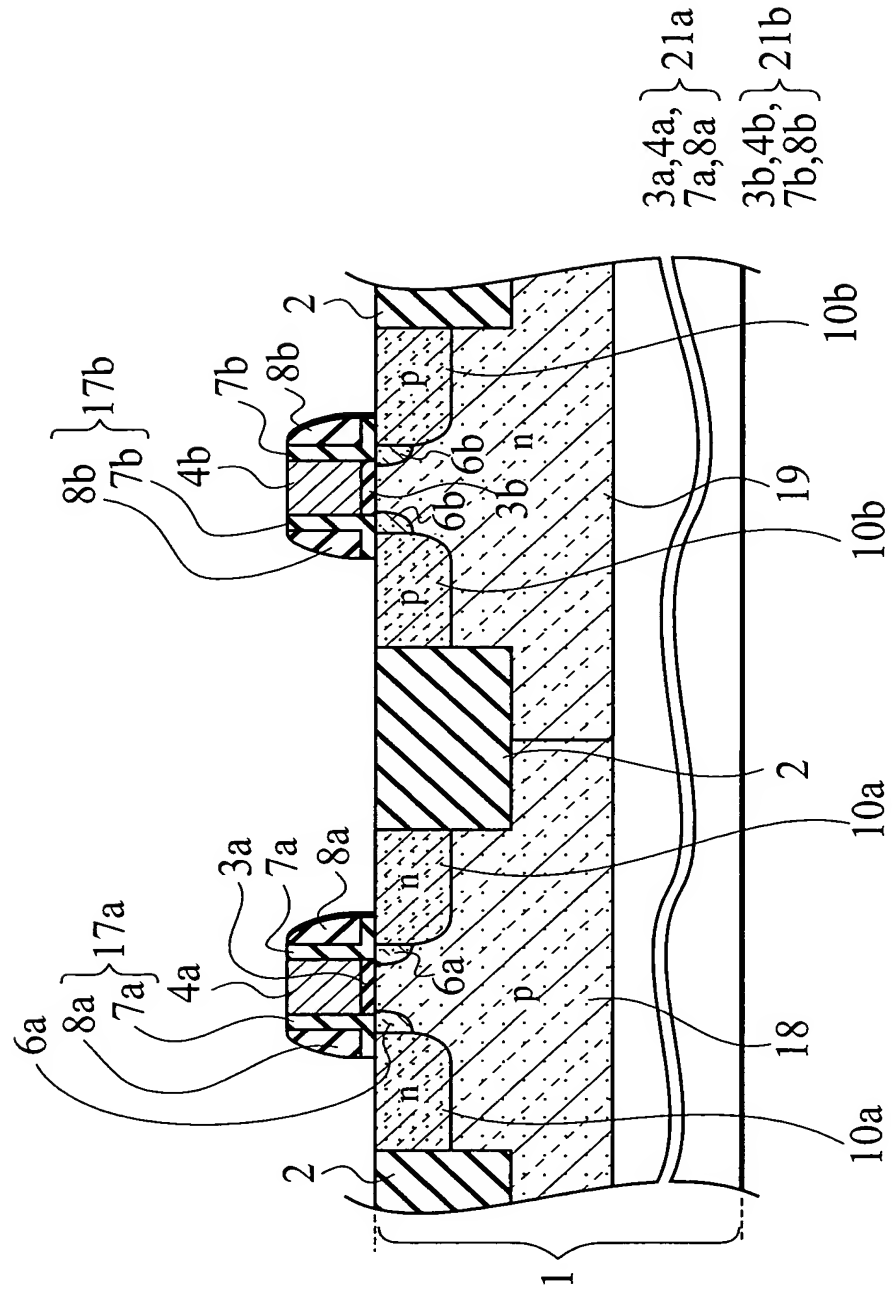


FIG. 1



A cross-sectional diagram of a semiconductor device. The structure consists of a substrate 1 with a wavy interface. Above the substrate is a layer 18. Within layer 18, there are two rectangular regions with diagonal hatching, labeled 2. The region between these two hatched regions is labeled 3. The region to the right of the second hatched region is labeled 19. The region to the left of the first hatched region is labeled 2. The region between the two hatched regions is labeled p, and the region to the right of the second hatched region is labeled n. A bracket on the left side of the diagram indicates the thickness of the substrate 1.

A cross-sectional diagram of a semiconductor device structure. The structure consists of a substrate 1 with a top layer 2. A central region 4 is defined by a top layer 2 and a bottom layer 3. A layer 18 is located between the top layer 2 and the central region 4. A layer 19 is located between the central region 4 and the top layer 2. The central region 4 is divided into two parts: a p-type region p and an n-type region n. The p-type region p is located on the left and the n-type region n is located on the right. The top layer 2 is shown with a dashed line indicating a boundary. The central region 4 is shown with a solid line indicating a boundary. The p-type region p is shown with a diagonal line pattern and the n-type region n is shown with a dotted line pattern. The substrate 1 is shown with a wavy line pattern. The top layer 2 is shown with a diagonal line pattern. The layer 18 is shown with a dashed line pattern. The layer 19 is shown with a dotted line pattern. The central region 4 is shown with a solid line pattern. The p-type region p is shown with a diagonal line pattern. The n-type region n is shown with a dotted line pattern. The substrate 1 is shown with a wavy line pattern.

FIG. 3A

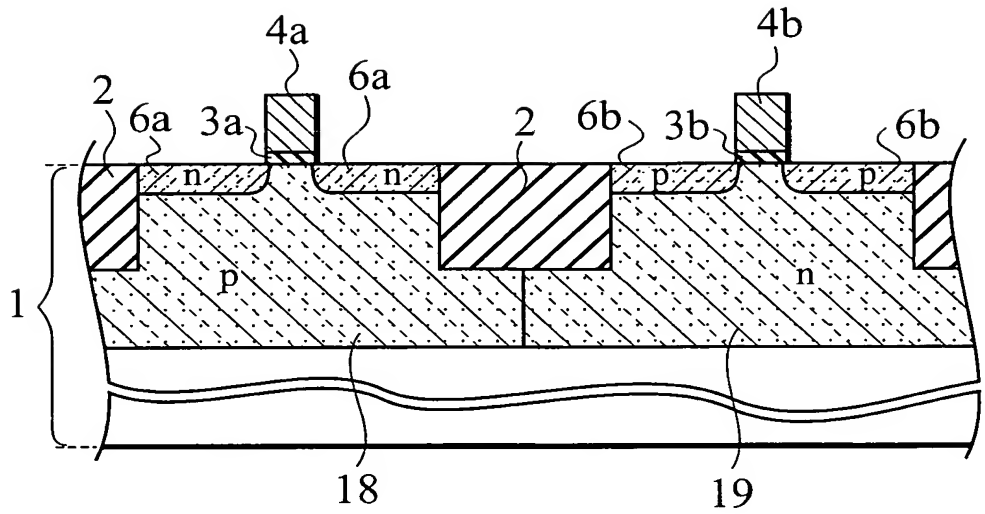
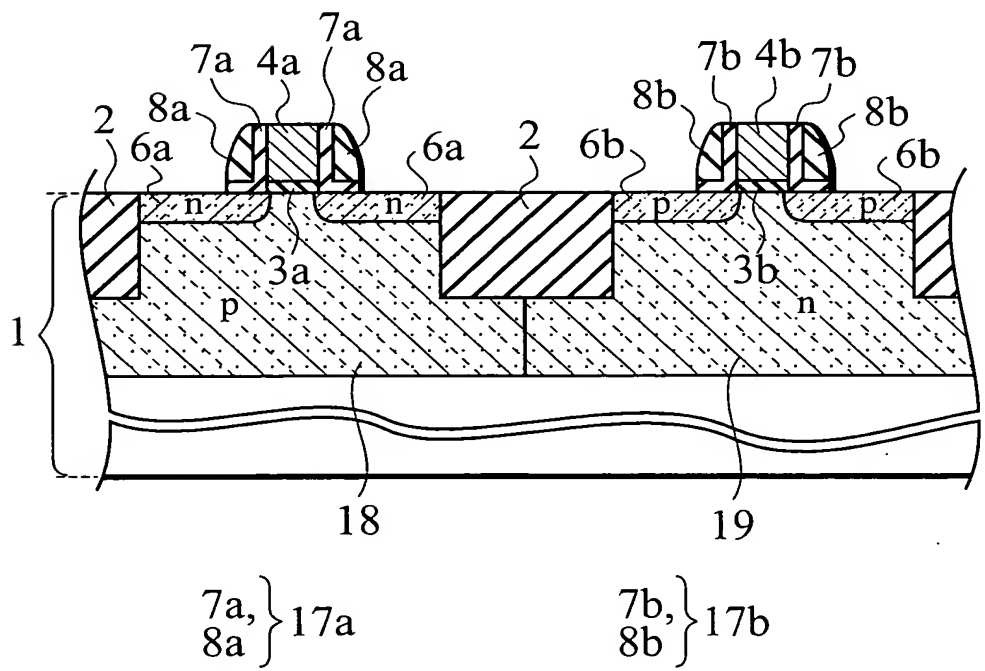


FIG. 3B



[illegible]

FIG. 5

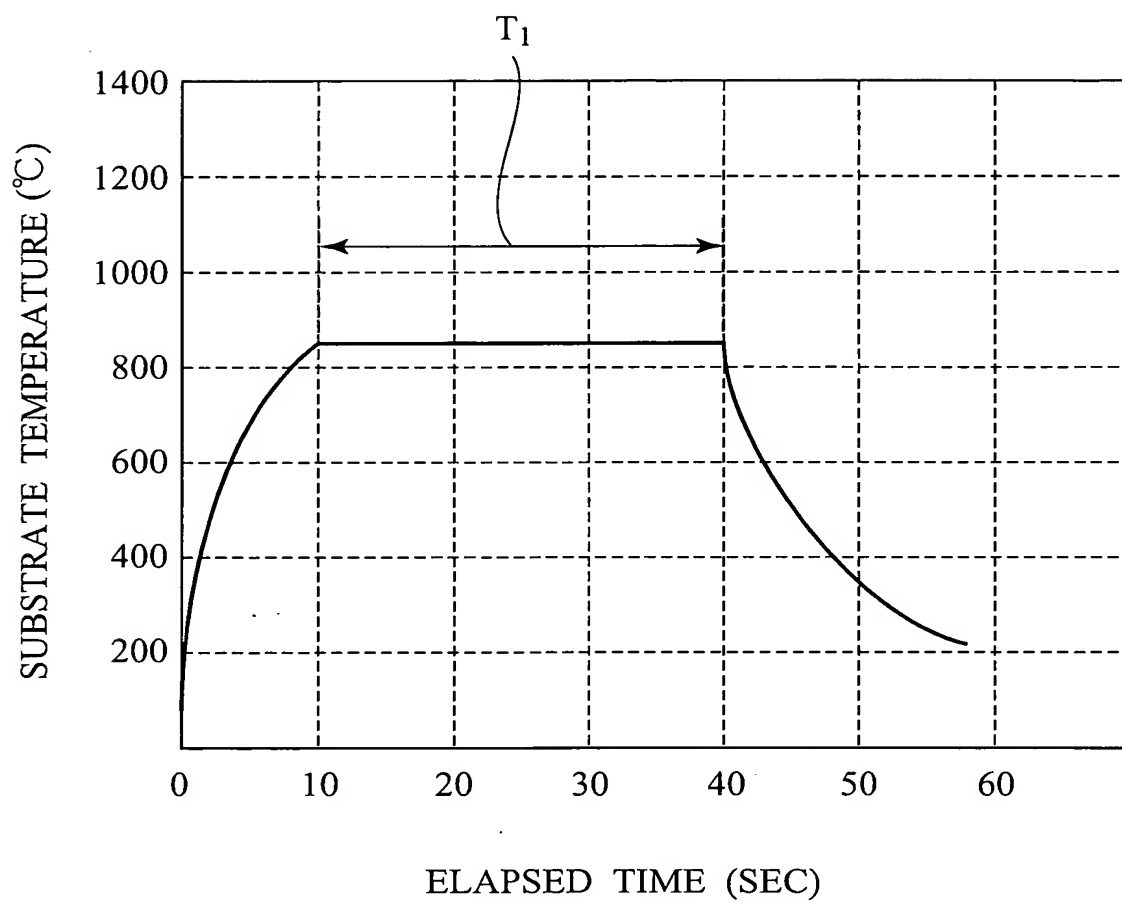


FIG. 6

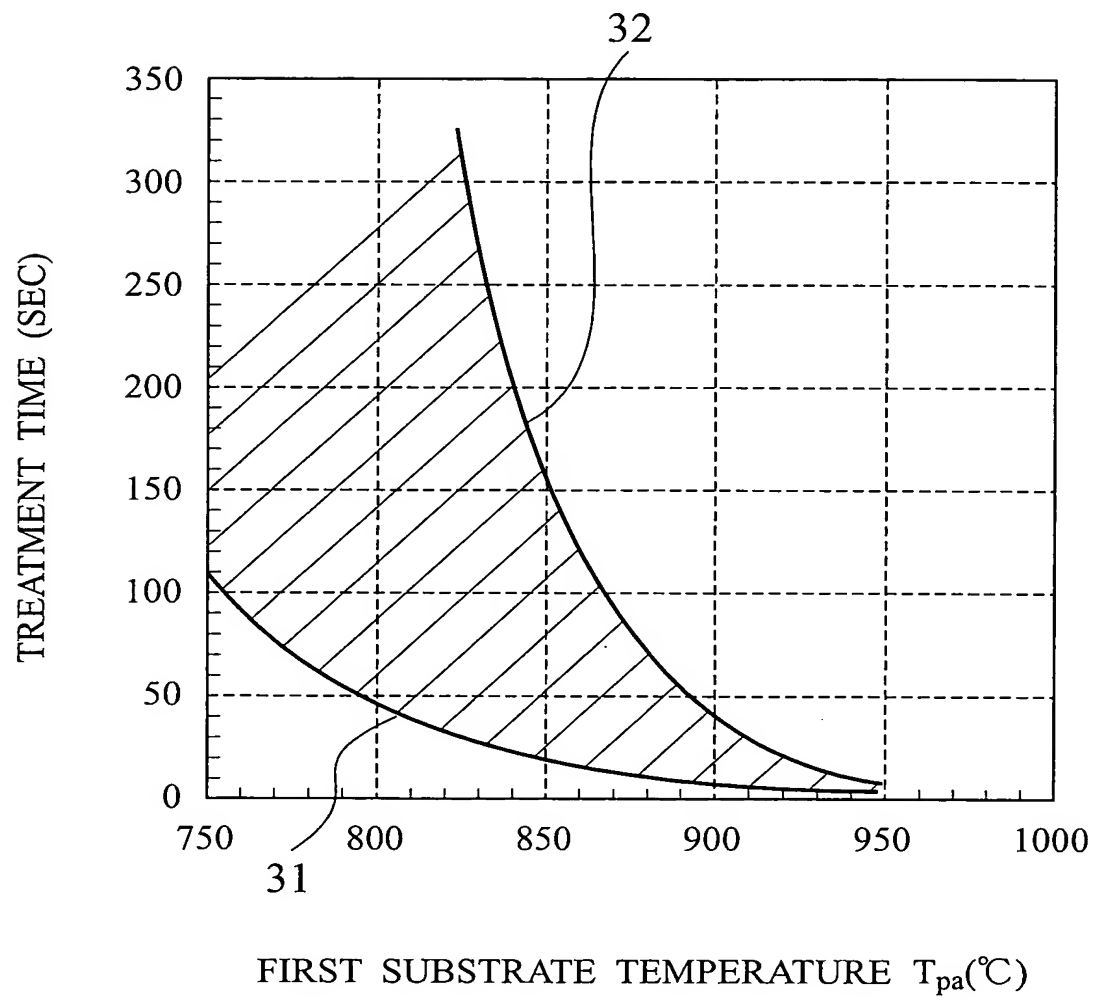


FIG. 7

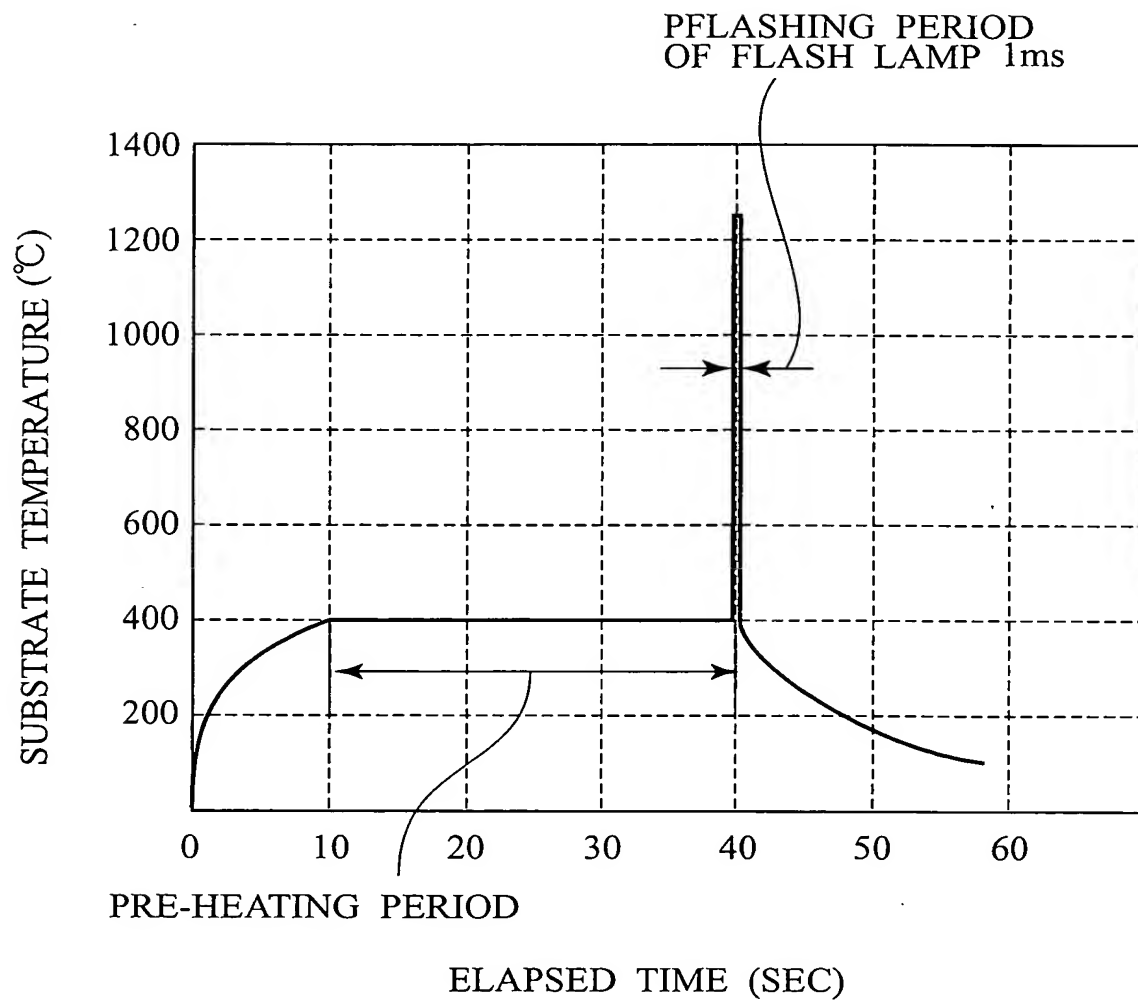


FIG. 8A

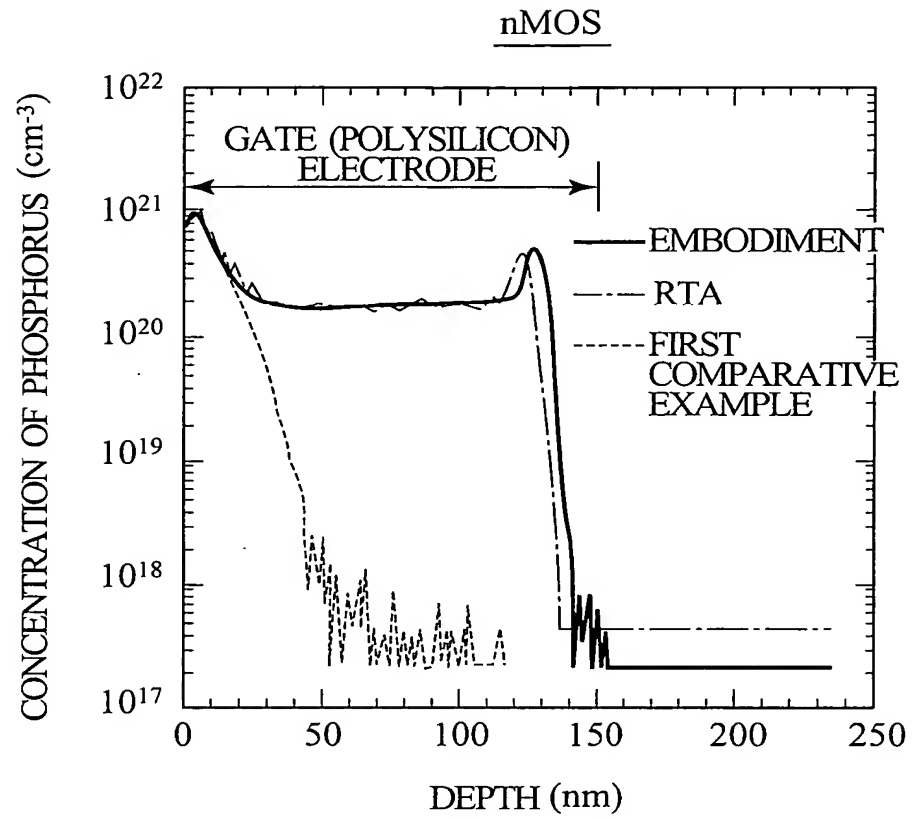
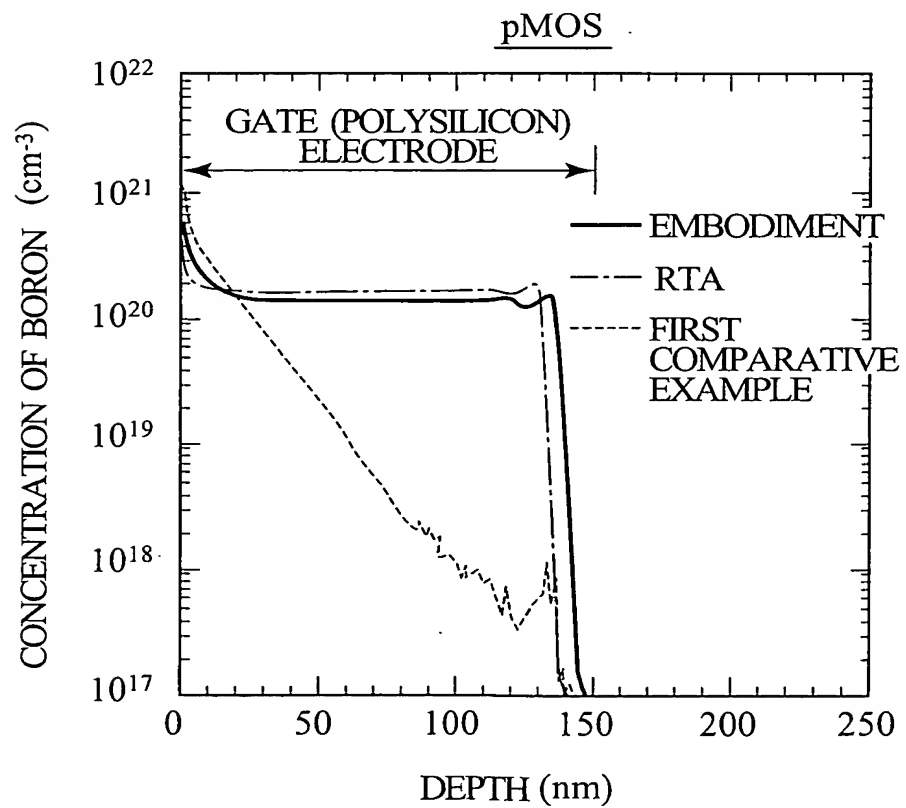


FIG. 8B





nMOS

FIG. 9A

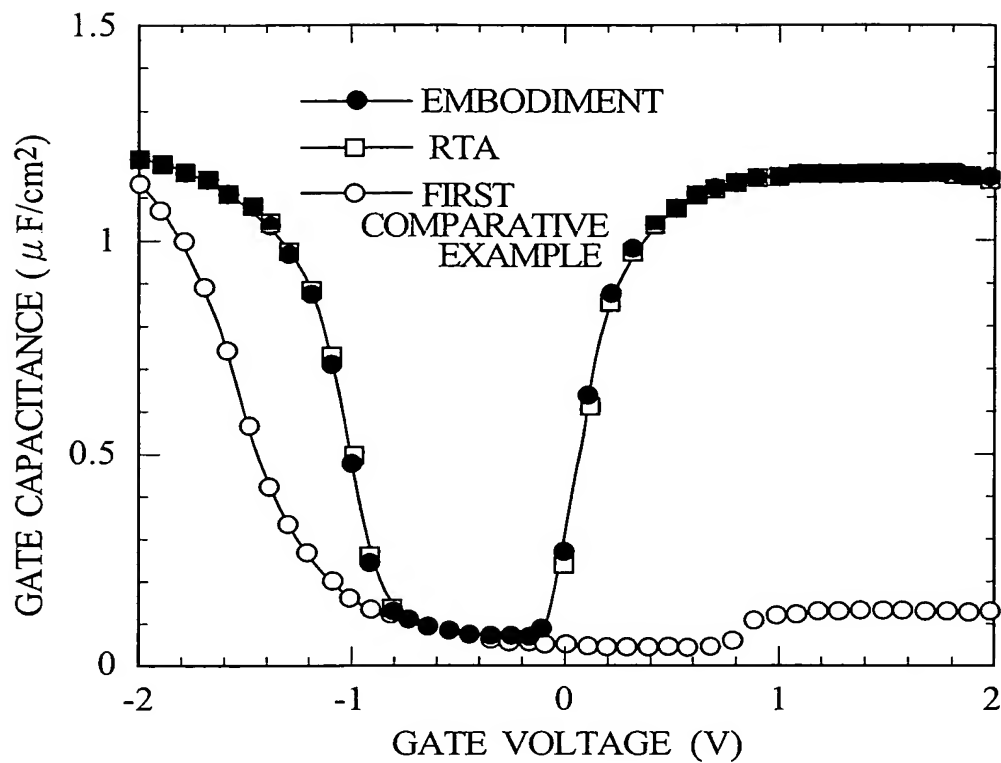
pMOS

FIG. 9B

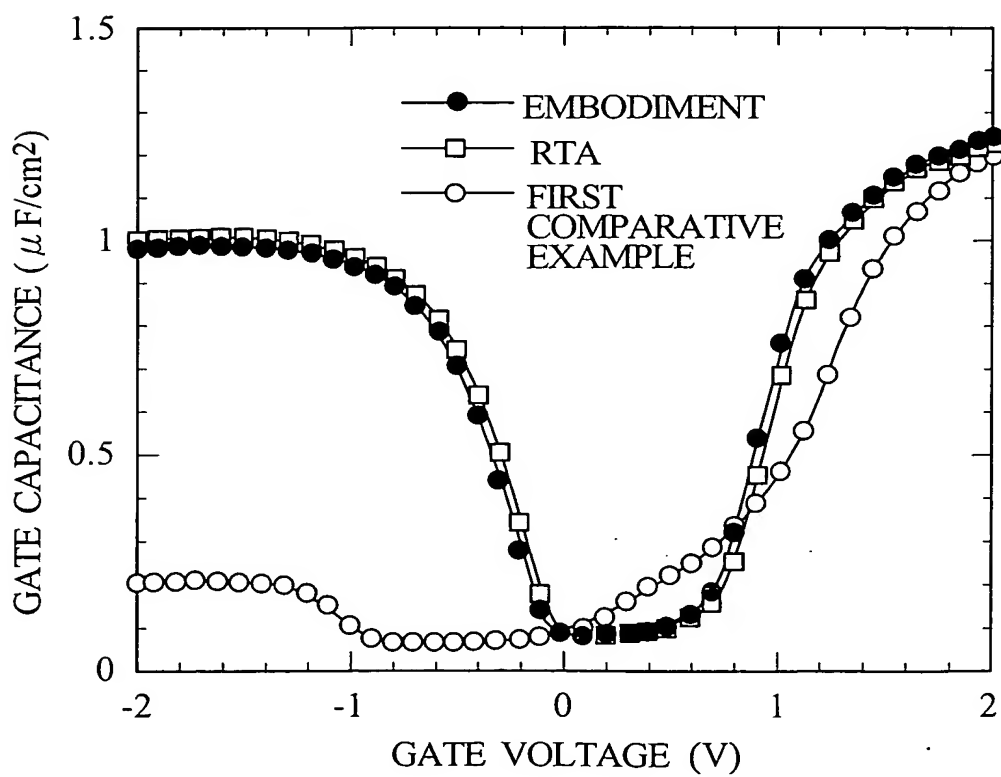


FIG. 10A

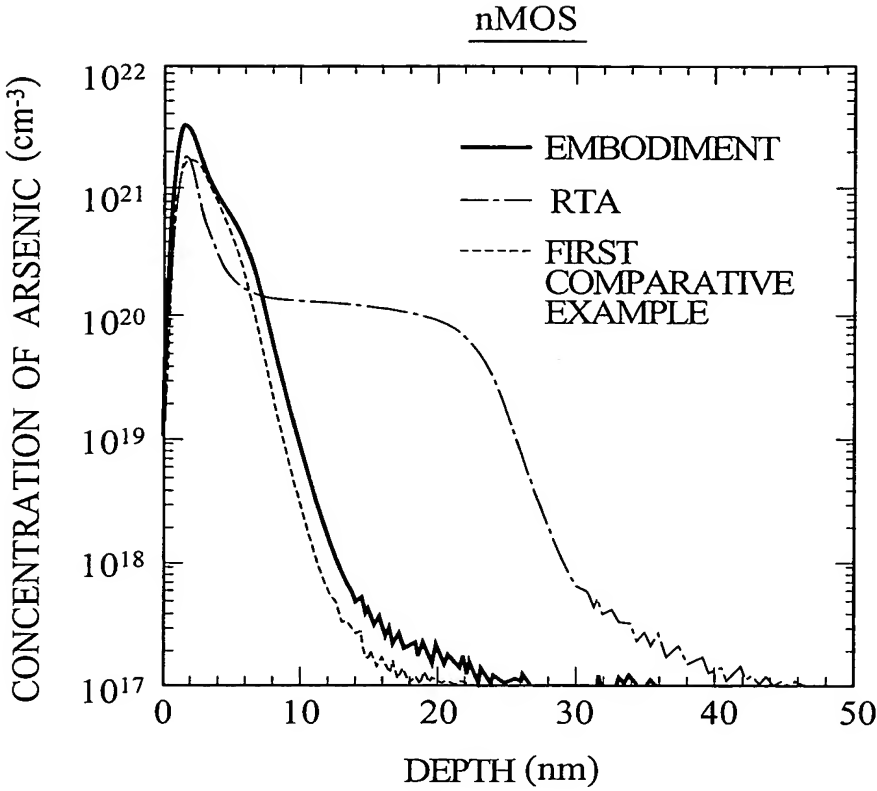


FIG. 10B

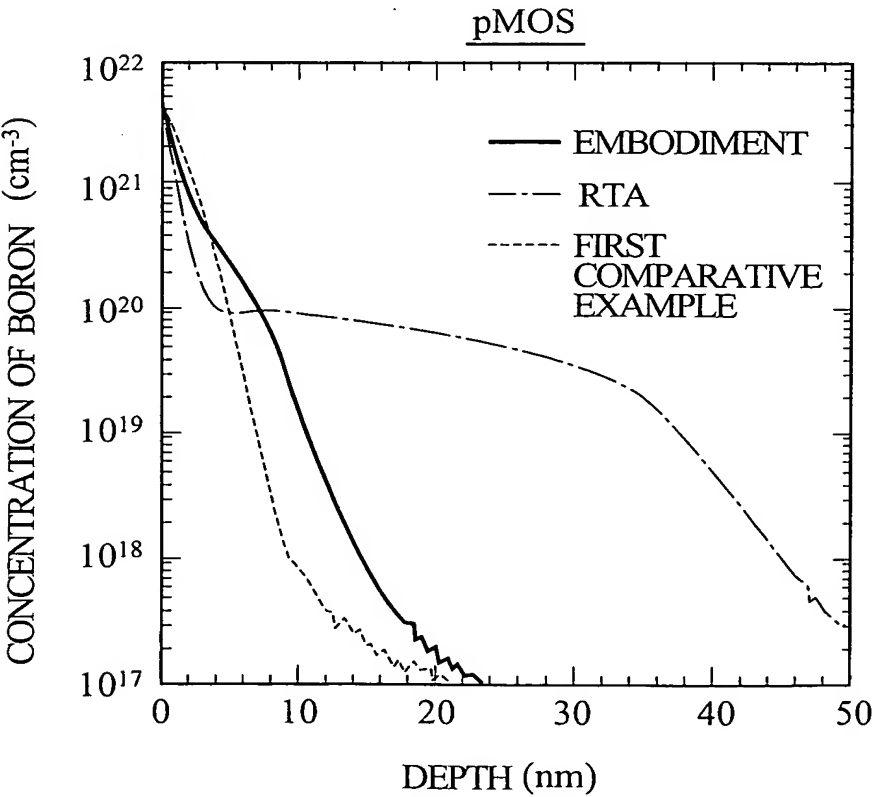


FIG. 11A

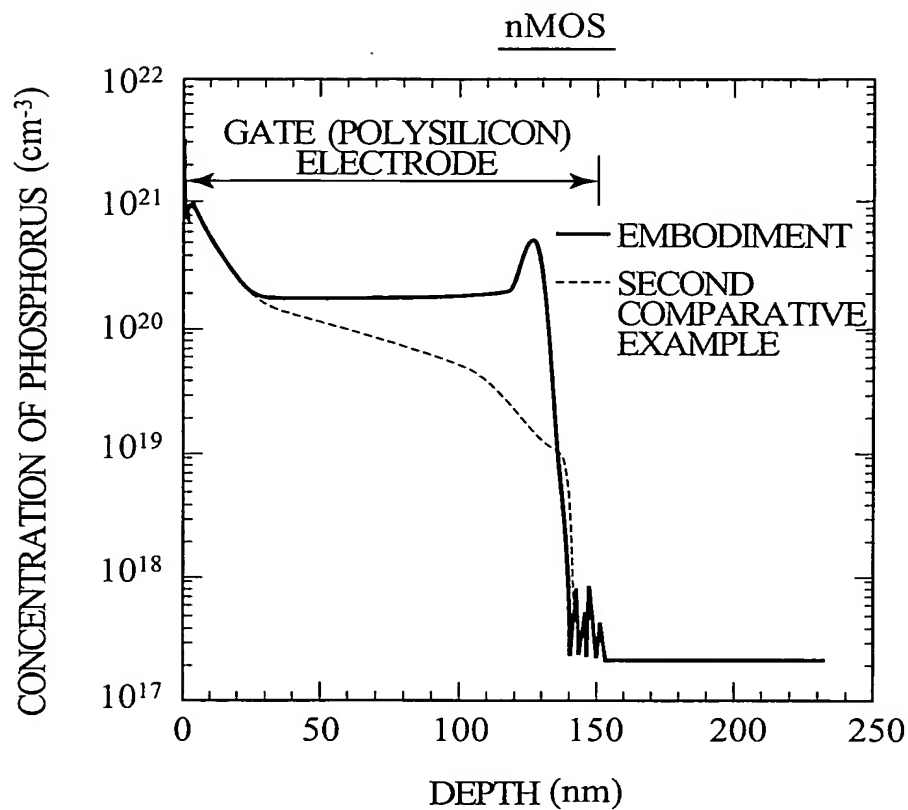
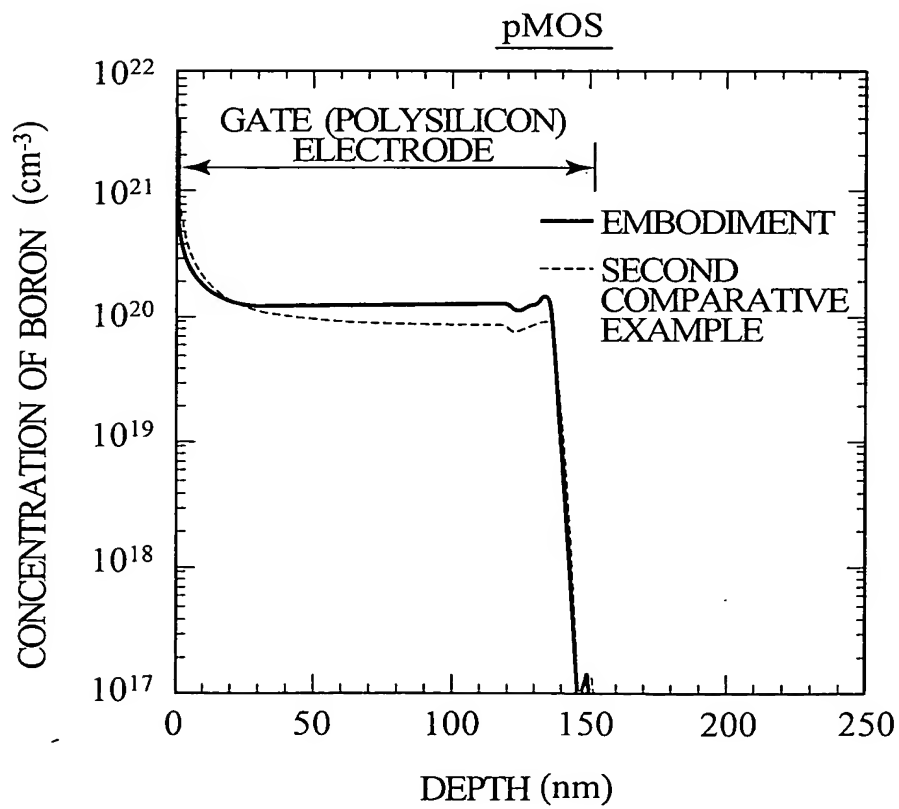


FIG. 11B



nMOS

FIG. 12A

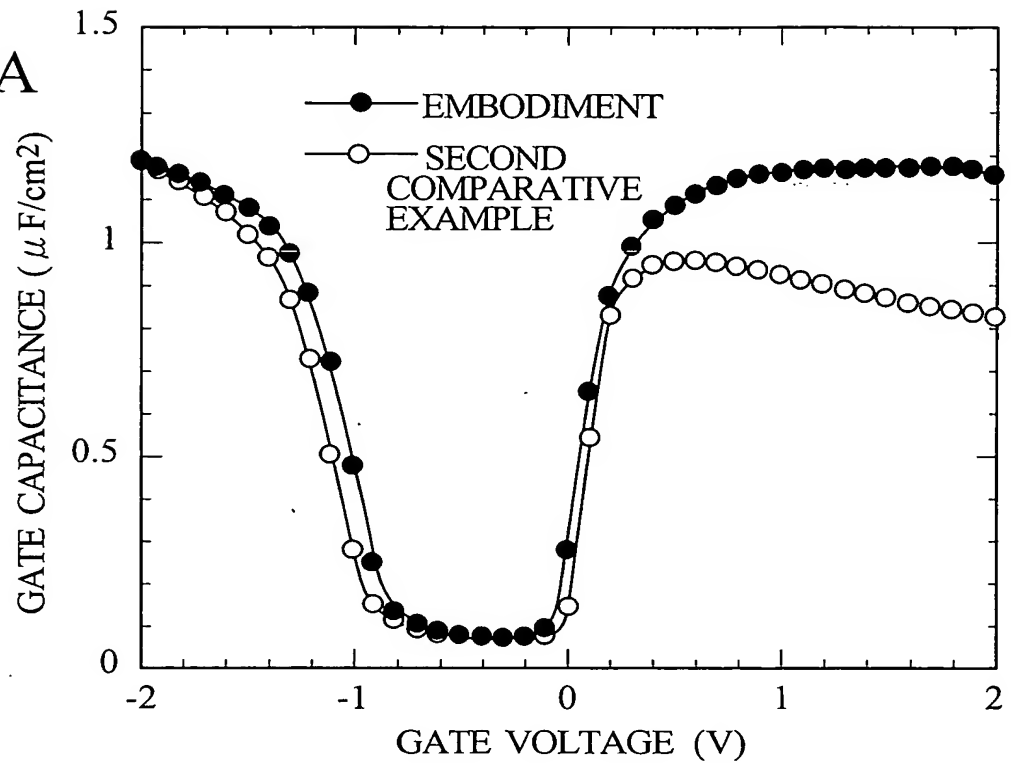
pMOS

FIG. 12B

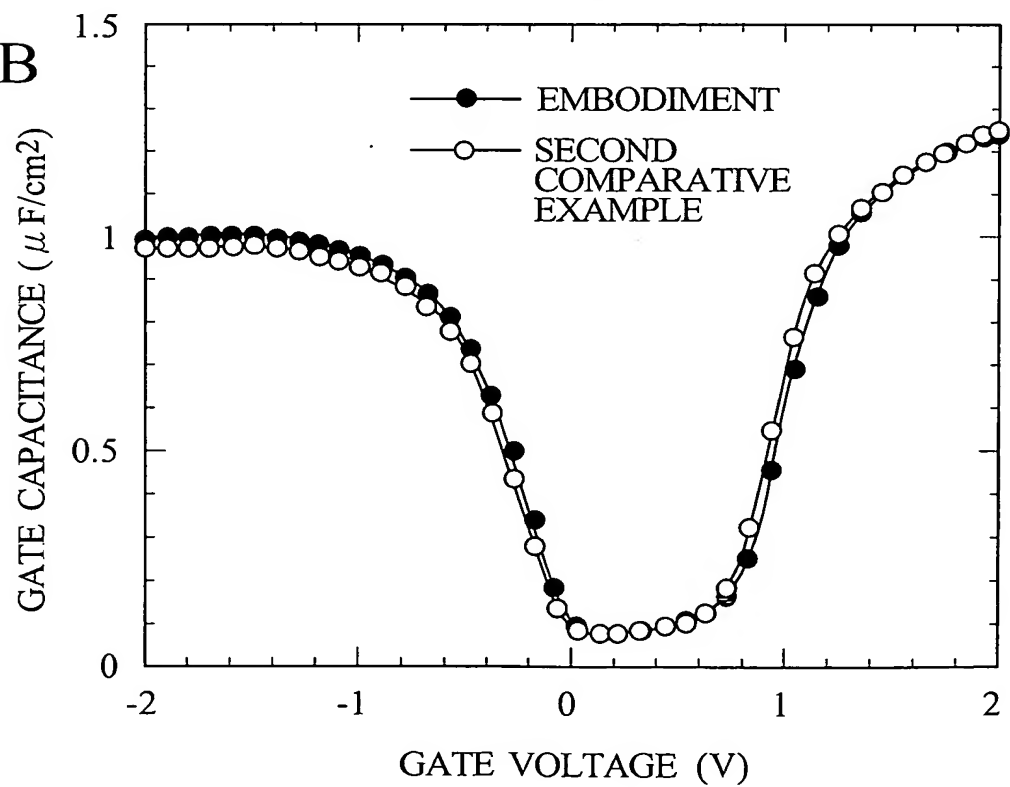


FIG. 13

